WHAT IS CLAIMED IS:

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1. A memory component with built-in self test, comprising: 2 an input/output interface coupled to the memory array and having a loopback; 3 a controller to transmit input/output test data to the input/output interface, and to 4 receive the input/output test data from the loopback of the input/output interface; and 5 a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output 6 7 interface. The memory component according to claim 1/wherein the memory component is 2. a dynamic random access memory (DRAM). 3. The memory component according to flaim 1, wherein the memory component is a buffer. 4. The memory component according to claim 3, wherein the buffer is an address <u>C</u>) 2 and command buffer. 1 5. The memory component according to claim 3, wherein the buffer is a data buffer. 6. 1 The memory component according to claim 3, wherein the buffer is an address 2 and command and data buffer.



- 7. The memory component according to faim 1, wherein the compare register
- 2 generates a test result based on the input/output test/data transmitted to the input/output interface
- 3 compared with the input/output test data received from the input/output interface.
- 1 8. The memory component according to claim 1, wherein the controller is adapted to
- 2 transmit memory array test data to a memory array to store the test data therein, and to read the
- 3 memory array test data from the memory array, and the compare register is adapted to compare
- 4 the memory array test data transmitted to the memory array with the memory array test data read
- 5 from the memory array.



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9. A memory component with built-in self test, comprising:

a memory array;

an input/output interface coupled to the memory array and having a loopback;

a controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array;

and

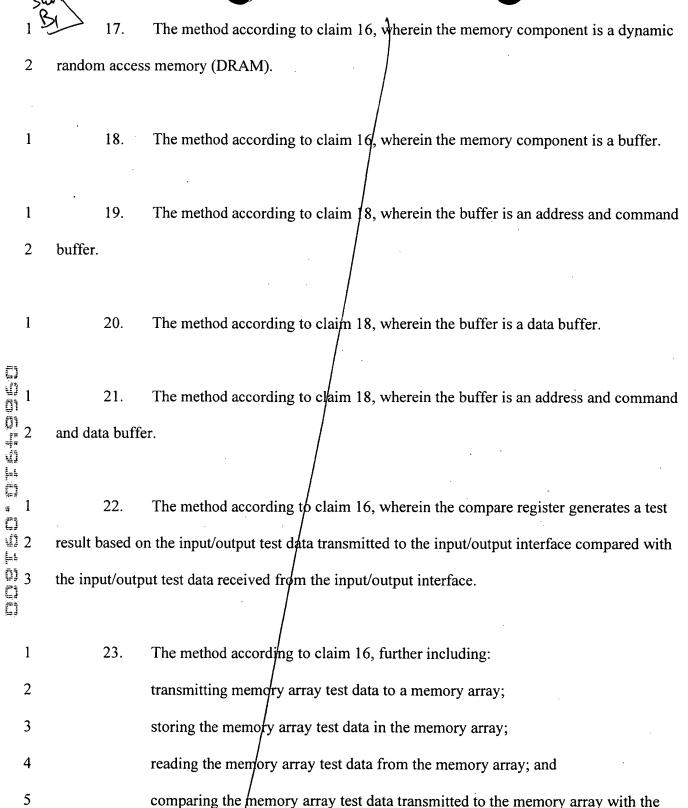
a compare register to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array.



- 10. The memory component according to claim 9, wherein the memory component is
- 2 a dynamic random access memory (DRAM).

the input/output test data received from the input/output interface.

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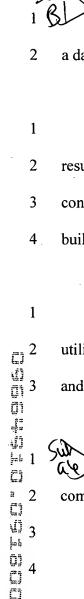


memory array test data read from the memory array.

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	1 -	ay)	24.	A method of testing a memory component with built-in self test, comprising:
The state of the s	2	- /		transmitting memory array test data to a memory array;
	3			storing the memory array test data in the memory array
	4			reading the memory array test data from the memory array; and
	5			comparing the memory array test data transmitted to the memory array with the
	6		memoi	ry array test data read from the memory array.
	1 St	R randon	25.	The method according to claim 24, wherein the memory component is a dynamic s memory (DRAM).
	1	buffer.	26.	The method according to claim 24, wherein the memory component is a buffer.
	1		27.	The method according to claim 26, wherein the buffer is an address and command
	1		28.	The method according to claim 26, wherein the buffer is a data buffer.
	1		29.	The method according to claim 26, wherein the buffer is an address and command
	2	2 and data buffer.		r. /
	1		30.	The method according to claim 24, wherein the compare register generates a test
	2	result b	ased or	the memory array test data transmitted to the memory array compared with the
	3	memor	y array	test data read from the memory array.

buffer includes an address and command generator to generate the address and command data.



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- 36. The memory module according to claim 31, wherein the test data is obtained from
- 2 a data bus through a memory controller.
- 1 37. The memory module according to claim 31, wherein the register receives the test
- 2 result from the at least one data buffer and reports the test result as one of the following
- 3 conditions: built-in self test not enabled, built-in self test enabled, built-in self test failed, and
- 4 built-in self test passed.
- 38. The memory module according to claim 31, wherein the at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from the at least one memory component.

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39. A method of testing a memory module with built-in self test, the method

comprising:

transmitting address and command/data and test data to a memory component

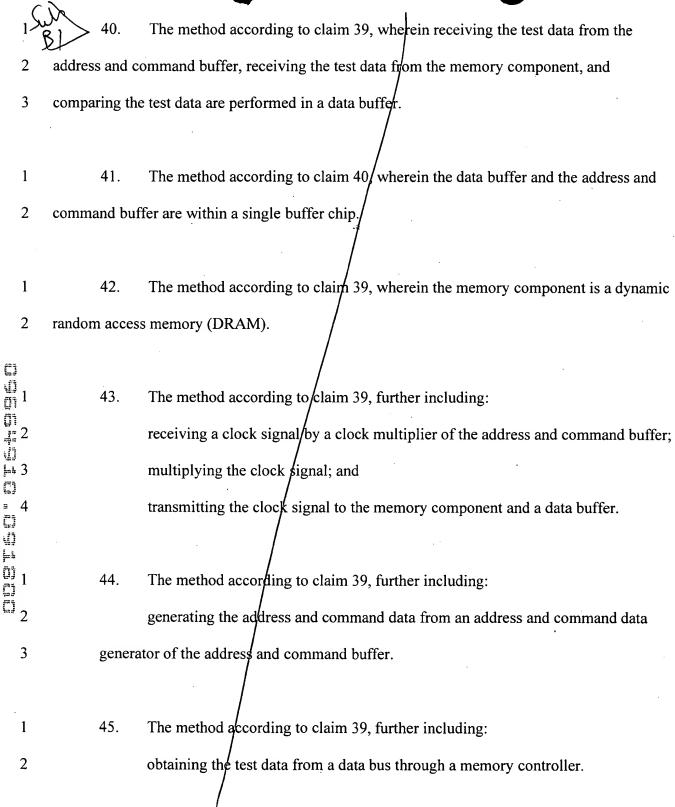
from an address and command buffer;

receiving the test data from the address and command buffer;

receiving the test data from the/memory component; and

comparing the test data received from the address and command buffer with the

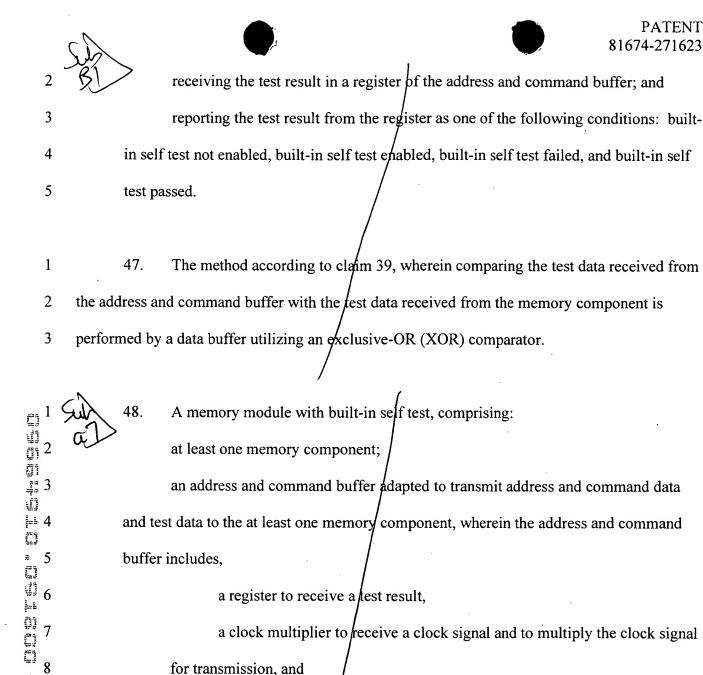
test data received from the memory/component to generate a test result.



The method according to claim 39, further including:

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data; and

at least one data buffer to receive the test data from the address and command buffer, to receive the test data from the at least one memory component, and to compare the test data received from the address and command buffer with the test data received from the at least one memory component to generate the test result.

an address and command generator to generate the address and command



- The memory module according to claim 48, wherein the address and command 49.
- buffer and the data buffer are within a single buffer chip. 2
- 1 50. The memory module according to claim 48, wherein the at least one memory
- component is a dynamic random access memory (DRAM). 2
- 1 51. The memory module acording to claim 48, wherein the test data is obtained from 2 a data bus through a memory controller.
 - 52. The memory module according to claim 48, wherein the register receives the test result from the at least one data buffer and reports the test result as one of the following conditions: built-in self test not knabled, built-in self test enabled, built-in self test failed, and built-in self test passed.
 - The memory/module according to claim 48, wherein the at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from the at least one memory component.

